Refine Search

Search Results -

Terms	Documents
L2 and (phase near3 free)	73

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 04, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and (phase near3 free)	73	L3
L2	(bus near3 phase) same (target or destination or receiver) same SCSI	139	L2
L1	(bus near3 phase) same ((target or destination or receiver) near3 comput$3) same SCSI	3	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 04, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and (phase near3 free)	73	L3
L2	(bus near3 phase) same (target or destination or receiver) same SCSI	139	L2
L1	(bus near3 phase) same ((target or destination or receiver) near3 comput$3) same SCSI	3	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
(L2 same (network or comput$3)) and (phase near3 free)	27

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L7

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 04, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L7	(L2 same (network or comput$3)) and (phase near3 free)	27	L7
L6	L2 same ((network or comput$3) and (phase near3 free))	19	L6
L5	l3 and (network or comput$3)	72	L5
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and (phase near3 free)	73	L3
L2	(bus near3 phase) same (target or destination or receiver) same SCSI	139	L2
L1	(bus near3 phase) same ((target or destination or receiver) near3 comput$3) same SCSI	3	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
(370/501 |370/492 |710/314 |710/72 |710/105 |710/113 |710/36 |710/315 |710/107 |710/119 |710/309 |710/305 |711/112 |712/1).ccls.	6740

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 04, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L1	710/314,72,105,113,36,315,107,119,309,305;370/501,492;711/112;712/1.ccls.	6740	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L3 and (comput$3 or network)	54

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 04, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L3 and (comput$3 or network)	54	L4
L3	l1 and L2	60	L3
L2	(bus near3 phase) same (target or destination or receiver) same SCSI	139	L2
L1	710/314,72,105,113,36,315,107,119,309,305;370/501,492;711/112;712/1.ccls.	6740	L1

END OF SEARCH HISTORY

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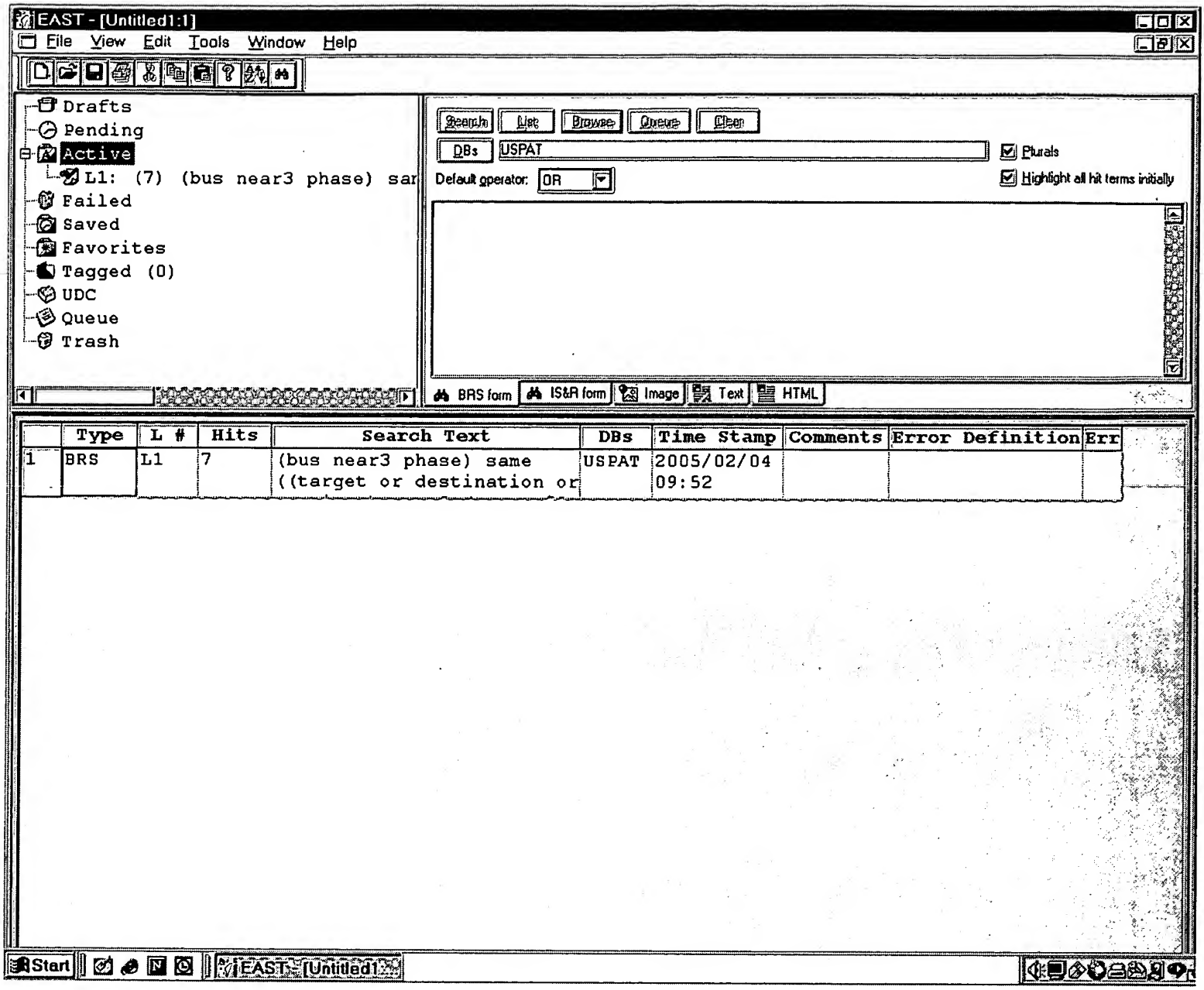
EAST - [Untitled1:1]
File View Edit Tools Window Help
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Active
L1: (7) (bus near3 phase) sar
Failed
Saved
Favorites
Tagged (0)
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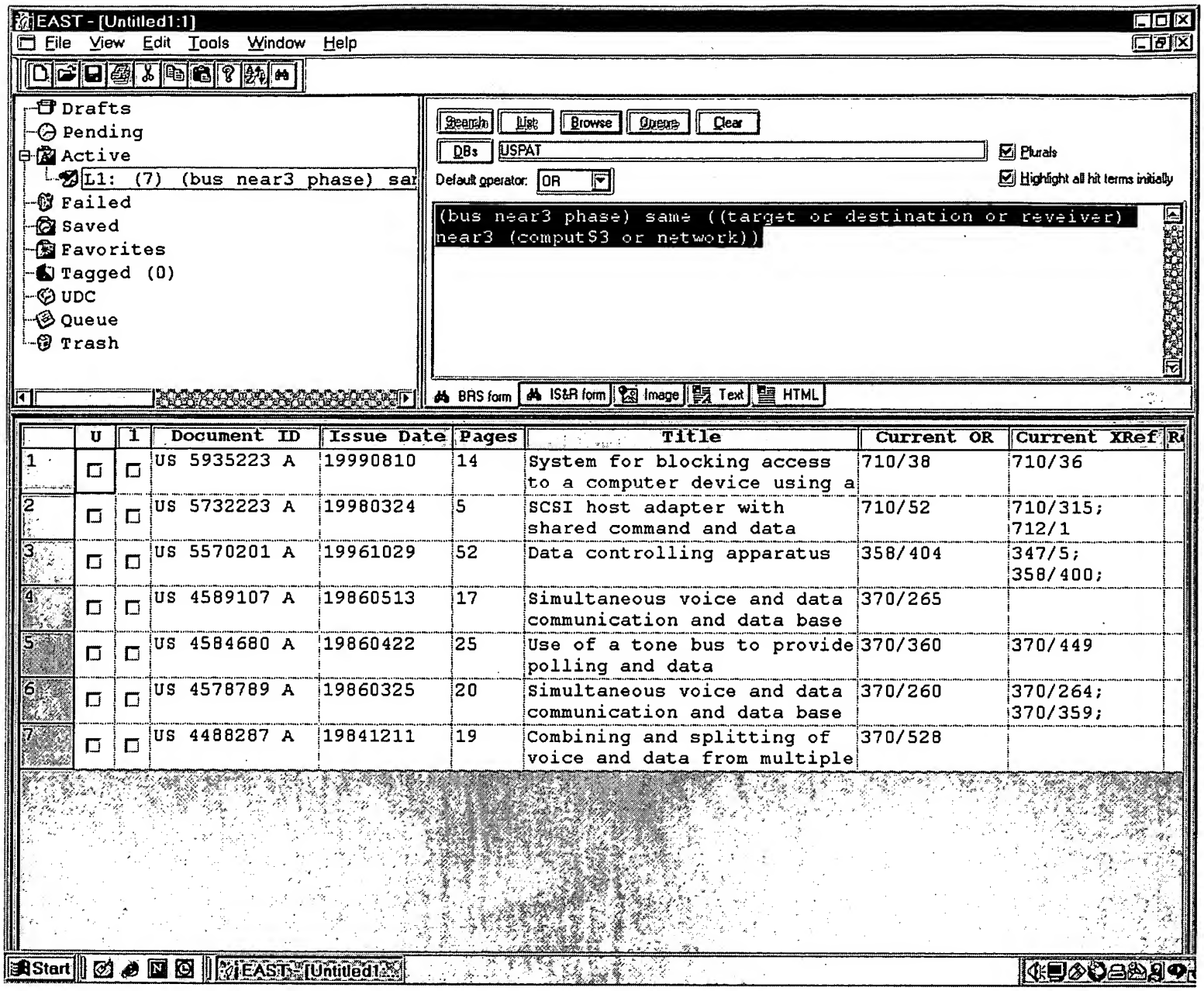
Queue
Trash
Search List Browse Queue Clear
DBs USPAT
Plurals
Default operator: OR
Highlight all hit terms initially
BRS form IS&R form Image Text HTML
Type L # Hits Search Text DBs Time Stamp Comments Error Definition Err
1 BRS L1 7 (bus near3 phase) same ((target or destination or USPAT 2005/02/04 09:52
Start
EAST - [Untitled1:1]



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 5935223 A	19990810	14	System for blocking access to a computer device using a	710/38	710/36	
2	☐	☐	US 5732223 A	19980324	5	SCSI host adapter with shared command and data	710/52	710/315; 712/1	
3	☐	☐	US 5570201 A	19961029	52	Data controlling apparatus	358/404	347/5; 358/400;	
4	☐	☐	US 4589107 A	19860513	17	Simultaneous voice and data communication and data base	370/265		
5	☐	☐	US 4584680 A	19860422	25	Use of a tone bus to provide polling and data	370/360	370/449	
6	☐	☐	US 4578789 A	19860325	20	Simultaneous voice and data communication and data base	370/260	370/264; 370/359;	
7	☐	☐	US 4488287 A	19841211	19	Combining and splitting of voice and data from multiple	370/528		

Your search matched **2** of **1123491** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

bus and phase and scsi Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **I/O issues in a multimedia system**
Narasimha Reddy, A.L.; Wyllie, J.C.;
Computer , Volume: 27 , Issue: 3 , March 1994
Pages:69 - 74

[Abstract] [PDF Full-Text (612 KB)] **IEEE JNL**

2 **A SEM-E module avionics computer with PI-Bus backplane communication**
Dougherty, M.J.;
Aerospace and Electronics Conference, 1990. NAECON 1990., Proceedings of t IEEE 1990 National , 21-25 May 1990
Pages:169 - 173 vol.1

[Abstract] [PDF Full-Text (412 KB)] **IEEE CNF**

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I/O issues in a multimedia system

Narasimha Reddy, A.L. Wyllie, J.C.
IBM Almaden Res. Center, San Jose, CA, USA;
This paper appears in: **Computer**

Publication Date: March 1994
On page(s): 69 - 74
Volume: 27 , Issue: 3
ISSN: 0018-9162
Reference Cited: 12
CODEN: CPTRB4
Inspec Accession Number: 4673959

Abstract:
In future computer system design, I/O systems will have to support continuous media such as video and audio, whose system demands are different from those of data such as text. Multimedia computing requires us to focus on designing I/O systems that can handle real-time demands. Video- and audio-stream playback and teleconferencing are real-time applications with different I/O demands. We primarily consider playback applications which require guaranteed real-time I/O throughput. In a multimedia server, different service **phases** of a real-time request are disk, small computer systems interface (**SCSI**) **bus**, and processor scheduling. Additional service might be needed if

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the request must be satisfied across a local area network. We restrict ourselves to the support provided at the server, with special emphasis on two service **phases**: disk scheduling and **SCSI bus** contention. When requests have to be satisfied within deadlines, traditional real-time systems use scheduling algorithms such as earliest deadline first (EDF) and least slack time first. However, EDF makes the assumption that disks are preemptable, and the seek-time overheads of its strict real-time scheduling result in poor disk utilization. We can provide the constant data rate necessary for real-time requests in various ways that require trade-offs. We analyze how trade-offs that involve buffer space affect the performance of scheduling policies. We also show that deferred deadlines, which increase buffer requirements, improve system performance significantly

Index Terms:

buffer storage file servers input-output programs multimedia systems peripheral interfaces real-time systems scheduling I/O issues **SCSI bus** contention computer system design constant data rate continuous media deferred deadlines disk scheduling earliest deadline first least slack time first local area network multimedia computing multimedia server multimedia system playback applications processor scheduling real-time I/O throughput real-time demands real-time request scheduling policies service **phases** small computer systems interface **bus** system demands

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A SEM-E module avionics computer with PI-Bus backplane communication

Dougherty, M.J.
Texas Instrum. Inc., Dallas, TX, USA ;

This paper appears in: **Aerospace and Electronics Conference, 1990. NAECON 1990., Proceedings of the IEEE 1990 National**

Meeting Date: 05/21/1990 - 05/25/1990
Publication Date: 21-25 May 1990
Location: Dayton, OH USA
On page(s): 169 - 173 vol.1
Reference Cited: 3
Inspec Accession Number: 3863903

Abstract:
The author describes the system architecture of a MIL-STD-1750A-based mission processor utilizing dual VHSIC **Phase** 2 TM-**Bus** and dual VHSIC **Phase** 2 PI-**Bus** for intermodule level communication. The mission processor consists of 18 surface-mount SEM-E modules and five high-density power supplies mating with an 18 layer G-10 backplane in an air-cooled chassis. The system-level interfaces consists of a dual PI-**Bus** for intermodule communication, a dual TM-**Bus** for intermodule operational test and maintenance, an IEEE-488 interface to an external software development platform, two

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differential small computer system interface (**SCSI**) buses, three dual redundant MIL-STD-1553B serial communication buses, and several digital and analog discrete I/Os. The author presents a comparison of the defined cycle sequence of each of the basic PI-**Bus** messages to the observed cycle structure of these message types in the system. The impact of chaining a sequence of PI-**Bus** messages is examined. Data on the impact of PI-**Bus** traffic on module performance under various conditions are examined

Index Terms:

VLSI aircraft instrumentation computer architecture computer interfaces microprocessor chips military equipment G-10 backplane IEEE-488 interface PI-**Bus** backplane communication PI-**Bus** traffic SEM-E module avionics computer Texas Instruments air-cooled chassis computer interfaces dual TM-**Bus** dual VHSIC **Phase** 2 TM-**Bus** dual redundant MIL-STD-1553B serial communication buses high-density power supplies intermodule communication mission processor surface-mount SEM-E modules system-level interfaces

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L4: Entry 48 of 54 File: USPT Jun 18, 1996

US-PAT-NO: 5528765
DOCUMENT-IDENTIFIER: US 5528765 A
**** See image for Certificate of Correction ****

TITLE: SCSI bus extension system for controlling individual arbitration on interlinked SCSI bus segments

DATE-ISSUED: June 18, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Milligan; James H.	Shoreview	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
R. C. Baker & Associates Ltd.	Burnsville	MN			02

APPL-NO: 08/ 031604 [PALM]
DATE FILED: June 15, 1993

INT-CL: [06] G06 F 13/36

US-CL-ISSUED: 395/287; 395/200.06, 370/85.2, 370/85.4, 364/240, 364/240.2, 364/242.6, 364/242.92, 364/DIG.1
US-CL-CURRENT: 710/107; 370/451, 370/462, 709/225, 709/249

FIELD-OF-SEARCH: 395/325, 395/275, 395/200, 395/200.06, 395/285, 395/287, 395/306, 395/308, 370/85.2, 370/85.4, 370/85.6, 340/825.5, 340/825.51

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4257095	March 1981	Nadir	395/325
☐	4320467	March 1982	Glass	395/301
☐	4620278	October 1986	Ellsworth et al.	395/325
☐	4706190	November 1987	Bomba et al.	395/325
☐	4961140	October 1990	Pechanek et al.	395/285
☐	5129090	July 1992	Bland et al.	395/725

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☐	5206946	April 1993	Brunk	395/500
☐	5237695	August 1993	Skokan	395/725
☐	5239651	August 1993	Sodos	395/725
☐	5265211	November 1993	Amini et al.	395/325
☐	5293493	March 1994	Smith et al.	395/325
☐	5317696	May 1994	Hilgendorf	395/325
☐	5345562	September 1994	Chen	395/275
☐	5412783	May 1995	Skokan	395/285
☐	5418914	May 1995	Heil et al.	395/293
☐	5440698	August 1995	Sindhu et al.	395/200.08
☐	5454111	September 1995	Frame et al.	395/288

ART-UNIT: 235

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Baker; Robert C. Proehl; Jeffrey A.

ABSTRACT:

This digital communication method and system permits extended distance communication on a SCSI bus despite the time constraints imposed on certain bus operations such as arbitration. The bus system is comprised of discrete bus segments each having a portal node and one or more devices interfaced thereon. All nodes are connected together by a serial link. Each node seizes control of its bus segment and imposes a pseudo-busy condition to prevent bus operations such as arbitration. A token message passed over the serial link between nodes allows one node at a time to release control of its segment to permit arbitration among the devices interfaced on its segment. A source device on the released segment that gains control of the segment as a result of arbitration may communicate with a destination device anywhere on the bus system.

37 Claims, 9 Drawing figures

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L1: Entry 1 of 2 File: USPT Nov 28, 2000

US-PAT-NO: 6154799
DOCUMENT-IDENTIFIER: US 6154799 A

TITLE: Repeater-switch for distributed arbitration digital data buses

DATE-ISSUED: November 28, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gafford; Thomas Austin	Redondo Beach	CA		
Eross, deceased; Botond Gabor	late of Palo Alto	CA		
Moorer, legal representative; by James A.	San Rafael	CA		
Barrie, legal representative; by Barbara L.	San Rafael	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Gafford; Thomas A.	Redondo Beach	CA			04

APPL-NO: 09/ 084163 [PALM]
DATE FILED: May 25, 1998

PARENT-CASE:
This is a continuation of application Ser. No. 07/923,996 filed Aug. 16, 1993, which issued May 26, 1998, as U.S. Pat. No. 5,758,109.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/107; 710/128, 710/129
US-CL-CURRENT: 710/107; 710/119

FIELD-OF-SEARCH: 710/107, 710/126, 710/127, 710/128, 710/129, 710/131, 710/100, 710/119

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4296469	October 1981	Gunter et al.	395/325

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☐	4604689	August 1986	Burger	364/200
☐	4716525	December 1987	Gilanyi et al.	364/200
☐	4821170	April 1989	Bernick et al.	364/200
☐	4864291	September 1989	Korpi	340/825.5
☐	5239632	August 1993	Larner	395/325
☐	5239653	August 1993	Cubero-Castan et al.	395/325
☐	5274783	December 1993	House et al.	395/325
☐	5337413	August 1994	Lui et al.	398/822
☐	5367647	November 1994	Coulson et al.	395/325
☐	5418914	May 1995	Heil et al.	395/293

OTHER PUBLICATIONS

United States Statutory Invention Registration No. H696, Oct. 3, 1989 Willard S. Davidson.
"OEMs Scramble to Launch Diverse SCSI Devices," Barry W. Phillips, Electronic Design, May 26, 1988, pp. 29-34.
"Intelligent Host Adapter Directs I/O Traffic, Freeing Up Host Processor," Robert Snively. Electronic Design, Sep. 20, 1984, pp. 243-252.
"Ethernet Controller Adds Communications to SCSI Bus," Tomas Russ, electronic Design, Sep. 8, 1988, pp. 91-96.
"American National Standard X3.131-1986," pp. 22-61.

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Chung-Trans; Xuong

ATTY-AGENT-FIRM: Schreiber; Donald E.

ABSTRACT:

The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed arbitration digital data buses (52, 54, 56, and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed arbitration buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed arbitration buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

13 Claims, 9 Drawing figures

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End of Result Set

☐ Generate Collection Print

L1: Entry 2 of 2 File: USPT May 26, 1998

US-PAT-NO: 5758109
DOCUMENT-IDENTIFIER: US 5758109 A

TITLE: Repeater/switch for distributed arbitration digital data buses

DATE-ISSUED: May 26, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gafford; Thomas Austin	Redondo Beach	CA		
Eross, deceased; Botond Gabor	late of Palo Alto	CA		
Morrer, co executor; James A.	San Rafael	CA		
Barrie, co executrix; Barbara L.	San Rafael	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Gafford; Thomas A.	Redondo Beach	CA			04

APPL-NO: 07/ 923996 [PALM]
DATE FILED: August 16, 1993

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/US90/01468	March 19, 1990	WO91/14989	Oct 3, 1991	Aug 16, 1993	Aug 16, 1993

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/308; 395/309
US-CL-CURRENT: 710/309

FIELD-OF-SEARCH: 395/325, 395/308, 395/309, 395/306, 395/299, 307/85.13, 307/85.6, 307/94.7

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4296469	October 1981	Gunter et al.	395/325
☐	4604689	August 1986	Burger	364/200

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☐	4716525	December 1987	Gilanyi et al.	364/200
☐	4821170	April 1989	Bernick et al.	364/200
☐	4864291	September 1989	Korpi	340/825.5
☐	5239632	August 1993	Larner	395/325
☐	5239653	August 1993	Cubero-Castan et al.	395/325
☐	5274783	December 1993	House et al.	395/325
☐	5367647	November 1994	Coulson et al.	395/325

OTHER PUBLICATIONS

United States Statutory Invention Registration No. H696, Oct. 3, 1989 Willard S. Davidson.
"OEMs Scramble to Launch Diverse SCSI Devices," Barry W. Phillips, Electronic Design, May 26, 1988, pp. 29-34.
"Intelligent Host Adapter Directs I/O Traffic, Freeing Up Host Processor," Robert Snively, Electronic Design, Sep. 20, 1984, pp. 243-252.
"Ethernet Controller Adds Communications to SCSI Bus," Tomas Russ, Electronic Design, Sep. 8, 1988, pp. 91-96.

ART-UNIT: 235

PRIMARY-EXAMINER: Ray; Gopal C.

ASSISTANT-EXAMINER: Chunk-Trans; Xuonk

ATTY-AGENT-FIRM: Schreiber; Donald E.

ABSTRACT:

The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed arbitration digital data buses (52, 54, 56, and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed arbitration buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed arbitration buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

14 Claims, 9 Drawing figures

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L7: Entry 2 of 27 File: PGPB Nov 11, 2004

PGPUB-DOCUMENT-NUMBER: 20040225824
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040225824 A1

TITLE: Network of computing devices including a repeater for distributed arbitration digital data buses

PUBLICATION-DATE: November 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Gafford, Thomas Austin	Redondo Beach	CA	US	
Eross, Botond Gabor	Palo Alto	CA	US	
Moorer, James A.	San Rafael	CA	US	

APPL-NO: 10/ 824072 [PALM]
DATE FILED: April 13, 2004

RELATED-US-APPL-DATA:
Application 10/824072 is a continuation-of US application 10/243537, filed September 14, 2002, ABANDONED
Application 10/243537 is a continuation-of US application 09/677853, filed October 3, 2000, ABANDONED
Application 09/677853 is a continuation-of US application 09/084163, filed May 25, 1998, US Patent No. 6154799
Application 09/084163 is a continuation-of US application 07/923996, filed August 16, 1993, US Patent No. 5758109
Application 07/923996 is a a-371-of-international WO application PC/T/US90/01468, filed March 19, 1990, PENDING

INT-CL: [07] G06 F 13/36

US-CL-PUBLISHED: 710/314
US-CL-CURRENT: 710/314

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed arbitration digital data buses (52, 54, 56 and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed arbitration buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be

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exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed arbitration buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

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L7: Entry 10 of 27 File: USPT Dec 1, 1998

US-PAT-NO: 5845154
DOCUMENT-IDENTIFIER: US 5845154 A

TITLE: System for supplying initiator identification information to SCSI bus in a reselection phase of an initiator before completion of an autotransfer command

DATE-ISSUED: December 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krakirian; Shahe H.	Milpitas	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Adaptec, Inc.	Milpitas	CA			02

APPL-NO: 08/ 463333 [PALM]
DATE FILED: June 5, 1995

PARENT-CASE:
This application is a division of application Ser. No. 08/205,002, still pending, filed Mar. 1, 1994.

INT-CL: [06] G06 F 13/00, G06 F 13/42

US-CL-ISSUED: 395/894; 395/800, 395/285, 395/309, 395/439, 395/825
US-CL-CURRENT: 710/74; 710/105, 710/5, 711/112

FIELD-OF-SEARCH: 395/325, 395/878, 395/285, 395/287, 395/281, 395/800, 395/309, 395/439, 395/825, 395/894, 364/238.3, 364/239, 364/248.1

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

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ART-UNIT: 237

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Chen; Anderson I.

ATTY-AGENT-FIRM: Skjerven, Morrill, MacPherson, Franklin and Friel Gunnison; Forrest E. Wallace; T. Lester

ABSTRACT:

A hard disk controller integrated circuit of a SCSI target device comprises a sequencer which causes a SCSI bus to transition from a command bus phase to a data transfer bus phase during execution of an autoread or an autowrite SCSI command without waiting for a communication from a microprocessor of the SCSI target

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device. In some embodiments, the command is determined to be either an autotransfer command or a non-autotransfer command. If the command is a non-autotransfer command, then the sequencer does not proceed directly to the data transfer phase but rather requires microprocessor intervention before proceeding to the data transfer phase. In some embodiments, an autotransfer command (such as an autoread or an autowrite command) is carried out by the disk drive controller integrated circuit with only two interrupts being generated to the microprocessor: one after receiving the autotransfer command from the initiator; and one after data transfer of the autotransfer command is complete. The hard disk controller integrated circuit automatically sends the status byte and command complete message if there is no queue tag collision as indicated by a cleared tag not okay flag.

3 Claims, 41 Drawing figures

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L7: Entry 21 of 27 File: USPT Mar 18, 1997

US-PAT-NO: 5613076
DOCUMENT-IDENTIFIER: US 5613076 A

TITLE: System and method for providing uniform access to a SCSI bus by altering the arbitration phase associated with the SCSI bus

DATE-ISSUED: March 18, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Latif; Farrukh	Malvern	PA		
Nguyen; Hung	Downington	PA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Unisys Corporation	Blue Bell	PA			02

APPL-NO: 08/ 352051 [PALM]
DATE FILED: November 30, 1994

INT-CL: [06] G06 F 13/36

US-CL-ISSUED: 395/293; 395/856, 395/859
US-CL-CURRENT: 710/113; 710/36, 710/39

FIELD-OF-SEARCH: 395/856, 395/859, 395/860, 395/865, 395/868, 395/731, 395/732, 395/734-737, 395/298-301, 395/893, 395/200.12, 395/200.13, 395/293, 395/294, 395/296

PRIOR-ART-DISCLOSED:

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ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Etienne; Ario

ATTY-AGENT-FIRM: Sterne, Kessler, Goldstein & Fox P.L.L.C.

ABSTRACT:

A host device SCSI bus controller in SCSI bus system for uniformly distributing I/O tasks, thereby providing all devices equal access to a SCSI bus without decreasing the overall utilization of the bus. The controller prevents system errors from occurring due to I/O tasks not being transmitted when the connectivity of the bus is fully utilized and the bus is operating near saturation. The controller alters the host device performance during the arbitration phase by replacing the single occurrence of the SCSI standard specified arbitration phase with multiple arbitration phases. In the multiple arbitration phases the controller does not assert the host device ID until a user determined time after the completion of the SCSI standard specified arbitration phase. When the host device has an I/O command to transmit, SCSI bus controller executes a first arbitration phase, wherein it does not assert the host device ID unless there are no reselecting target devices and not until a user defined time after the SCSI standard specified arbitration delay has completed. This gives a reselecting target device the opportunity to gain control over the SCSI bus. Then, if there are additional reselecting target devices on the SCSI bus, the SCSI bus controller performs additional arbitration phases until the bus is free. At that time, the SCSI bus controller issues the pending I/O command. By delaying the assertion of the host device ID during repeated arbitration phases, the SCSI bus controller enables the remaining target devices the opportunity to sequentially gain control over the SCSI bus. The SCSI bus controller therefore allows all target devices to reselect the host device to complete previously issued I/O tasks prior to the host device issuing additional I/O commands. The SCSI bus controller allows for an exception when a host I/O command is delayed to such an extent that further delay will cause a system error. Under such conditions, the SCSI bus controller asserts the host ID during the next standard arbitration phase. The host will then win arbitration and transmit the critical I/O command.

11 Claims, 14 Drawing figures

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US005732223A

United States Patent [19]

Moore et al.

[11] Patent Number: 5,732,223

[45] Date of Patent: Mar. 24, 1998

[54] **SCSI HOST ADAPTER WITH SHARED COMMAND AND DATA BUFFER**

[75] Inventors: Richard S. Moore, Irvine; David J. O'Shea, Newport Beach, both of Calif.

[73] Assignee: Future Domain Corporation, Inc., Irvine, Calif.

[21] Appl. No.: 963,584

[22] Filed: Oct. 20, 1992

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 667,754, Mar. 11, 1991, abandoned.

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/250; 395/800

[58] Field of Search 395/325, 375, 395/800, 280, 292, 474, 250

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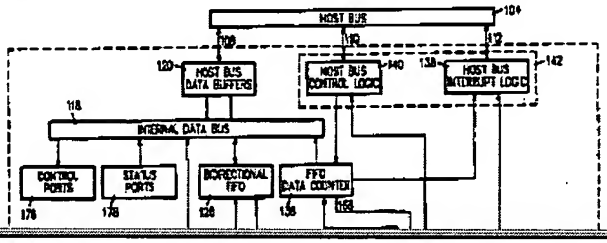
Primary Examiner—William M. Treat
Assistant Examiner—Zarni Maung
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel, LLP

[57] ABSTRACT

A small computer system interface (SCSI) controller circuit, connected between a host computer bus and a SCSI bus, includes a storage buffer shared between command and data signals provided by a host computer to a target SCSI peripheral device. The shared buffer includes a bidirectional FIFO which is used for intermediate storage of command blocks between transferred the host and the target device as well as data blocks. In the case of data transfers from the host to the target device, a command block is written to the bidirectional FIFO followed by as much of the data block as will fit in the remaining FIFO space. After the target device has read the command block, it accesses the SCSI bus and begins the transfer of data from the FIFO. In the case of data transfers from the target device to the host, a data transfer command block is first written to the FIFO by the host. The command block is read by the target device which then provides the requested data to the FIFO over the SCSI bus. The host system receives the requested data from the same shared storage buffer to which the command block was written.

15 Claims, 1 Drawing Sheet



United States Patent [19]
Carter et al.

[11] **Patent Number: 4,488,287**
[45] **Date of Patent: Dec. 11, 1984**

[54] **COMBINING AND SPLITTING OF VOICE AND DATA FROM MULTIPLE TERMINAL SOURCES AND ELECTRONIC PABX FOR SAME**

[75] Inventors: Nicholas J. R. Carter, Shelton; Francisco A. Middleton, Sandy Hook; Santana Das, Shelton, all of Conn.

[73] Assignee: International Telephone and Telegraph Corporation, New York, N.Y.

[21] Appl. No.: 443,626

[22] Filed: Nov. 30, 1982

[51] Int. Cl.³ H04Q 11/04
[52] U.S. Cl. ..... 370/58; 179/2 DP
[58] Field of Search ..... 370/85, 58, 110.1; 179/2 DP

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Primary Examiner—Douglas W. Olms
Assistant Examiner—Wellington Chin
Attorney, Agent, or Firm—John T. O'Halloran; Jeffrey P. Morris

[57] **ABSTRACT**

The present invention discloses a data partitioning technique wherein the PCM speech transmission data field is utilized to contain both digitized speech (for example, from a telephone) and other data (for example, from a data terminal) in the same channel within a frame having a plurality of channels e.g. 32 channels, of information. This enables the speech and data to be combined in a common information field and simultaneously transmitted in the same channel, frame by frame, through a digital switching network to other system users. Also, in accordance with the present invention, system users can individually selectively access a data base system through the switching network, such that the same information can be broadcast from the database system to a plurality of system users, or such that different information can be accessed in the database system by a plurality of system users and simultaneously transmitted to different users in different channels. A novel technique for transmitting information from the database system via a telecommunication systems tone bus interconnecting the system is described.

38 Claims, 11 Drawing Figures